REMARKS

This Amendment is filed in response to the Final Office Action dated August 9, 2005, which has a shortened statutory period set to expire November 9, 2005.

Jarwala: Overview

Jarwala teaches a test system 10 that can test a plurality of circuit boards 12. Col. 2, lines 64-66. Each circuit board has a Boundary Scan architecture, wherein each Boundary Scan cell comprises a single-bit register associated with an electronic component 15, such as an integrated circuit. Col. 3, lines 1-2 and 8-11. Actual testing of circuit boards 12 is carried out by a Boundary Scan Master Virtual Machine (BVM) 17 that includes an interpreter 18 and a plurality of Boundary Scan Masters (BSM) 20, wherein each BSM 20 controls the testing of a circuit board 12. Col. 3, lines 37-45.

Test system 10 includes a system test and diagnosis host 16 that initiates testing and diagnosis without regard to the specific nature of the board 12 to be tested. Col. 2, lines 29-32. BVM 17 interprets a testing command from host 16 and communicates to each board 12 at least one command that causes board 12 to commence testing with a test program specific to that board 12. Col. 2, lines 32-38. Each BSM 20 includes a process and a set of registers for executing that test program and to provide the results of such testing to interpreter 18 (of BVM 17). Col. 2, lines 40-44. BVM 17 enables host 16 to manage testing without concern as to the specific details of the boards 12 under test.

Claims 7-13 and 17-20 Are Patentable Over The Cited References

Applicant respectfully traverses the rejection of Claims 7-13. Specifically, Claim 7 recites:

An integrated circuit testing system comprising:

a) an integrated circuit tester comprising:

a1) a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random; and

a2) a second memory for storing therein deterministic test vector data, said first and second memory coupled to a port;

b) an integrated circuit device under test (DUT) comprising:

b1) a circuit block to be tested;

b2) a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number; and

b3) a selector circuit coupled to said port and for generating a test vector for application to said circuit block, said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

Applicants respectfully submit that Jarwala fails to disclose or suggest the recited IC tester and IC DUT. The Office Action states that TVO memory 32, ATPG 34, and multiplexer 36 teach the recited second memory, random number generator, and selector circuit, respectively. Applicants traverse this characterization. Specifically, as recited in Claim 7, the random number generator and the selector circuit are included on the integrated circuit device under test (IC DUT). In contrast, Jarwala teaches testing a circuit board 12, wherein each circuit board 12 includes a plurality of electrical

components 15, such as ICs. Therefore, Jarwala fails to teach the recited IC DUT.

The Office Action admits that Jarwala fails to explicitly disclose the first memory that stores a mask vector. Moreover, as recited in Claim 7, the first and second memories are included on an IC tester. The Office Action ignores this limitation. Notably, the separation of components between the IC tester and the IC DUT provides significant advantages.

Specifically, as taught by Applicants in reference to Figure 3, which illustrates an exemplary implementation:

> The system of Figure 3 acts to reduce the throughput of the data flowing from the tester 14' to the DUT 16'. The embodiment of Figure 3 reduces the tester throughput to the DUT 16' by incorporating the LFSR circuit 230 on the DUT 16' itself. A configurability mechanism for sending data from the tester 14' or the compressed data source on the DUT 16' can be built-in. The control of the source of test data to the design would lie in the hands of the control logic 250 of the tester 14'. The embodiment of Figure 3 also offers an increase in performance. Specifically, this configuration allows for the possibility of obtaining and applying the data portion that is generated on the DUT 16' at a faster rate than that could be achieved from a low cost tester.
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> Specification, page 20, lines 4-13.

Because Jarwala fails to teach the IC tester and the IC DUT, Jarwala cannot achieve the tester throughput and the performance provided by Applicants' recited testing system. Because Jarwala fails to disclose or suggest the recited testing system, Applicants request reconsideration and withdrawal of the rejection of Claim 7.

Claims 8-13 depend from Claim 7 and therefore are patentable for at least the reasons presented for Claim 7.

Moreover, with respect to Claims 11 and 12, Lesmeister fails to remedy the deficiencies of Jarwala. Based on all of the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 8-13.

Claim 17 recites:

> A method for testing an integrated circuit comprising the steps of:
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> a) retrieving a mask vector from a first memory, said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random;
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> b) retrieving deterministic test vector data from a second memory;
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> c) initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number;
>
> d) generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector
>
> e) applying said output test vector to said circuit block;
>
> f) obtaining an output generated by said circuit block in response to said output test vector; and
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> g) supplying said output generated by said circuit block to an input of a stage of said random number generator.

Applicants respectfully submit that Jarwala fails to disclose or suggest the recited step of supplying the output generated by the circuit block to an input of a stage of the random number generator (i.e. step g)). As taught by Applicants in reference to Figure 4B, which illustrates an exemplary implementation:

> Figure 4B illustrates another embodiment of the LFSR circuit 230b which 5 can interleave output values from the DUT 16 using OR gates 320-322. By interleaving the output values (e.g., over output lines 330-332) into the LFSR 230b, the effective "randomness" of the result is increased. This also increases error detection because an error on the output lines 330-332 will generate an improper input test pattern which will likely lead to another departure from the expected result on the output, etc. This increases the likelihood that the error is detected by the verification circuitry 240 (Figure 2, Figure 3). The output lines 330-332 originate from the output of the DUT 16. The value of line 330 is ORed into the output of the first stage 310. The value of line 331 is ORed into the output of the second stage 311. The value of line 332 is ORed into the output of the third stage 312. It is appreciated that any number of stages can be used in accordance with this embodiment of the present invention.
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> Specification, page 22, lines 4-16.

In contrast, Jarwala fails to teach supplying the output generated by the circuit block to an input of a stage of the random number generator. The Office Action characterizes the Test Vector Manipulation register (of BSM internal registers 29) as being the recited circuit block. Applicants traverse this characterization. Specifically, the output test vector is applied to a circuit block of the integrated circuit. Therefore, the recited circuit block cannot be taught by the Test Vector Manipulation register of Jarwala.

Because Jarwala fails to teach supplying the output generated by the circuit block to an input of a stage of the random number generator, Jarwala cannot achieve the effective "randomness" provided by Applicants' recited method. Because Jarwala fails to disclose or suggest the recited method, Applicants request reconsideration and withdrawal of the rejection of Claim 17.

Claims 18-20, as amended, now depend from Claim 17 and therefore are patentable for at least the reasons presented for Claim 17. Moreover, with respect to Claim 18, Lesmeister fails to remedy the deficiencies of Jarwala. Based on all of the above reasons, Applicants request reconsideration and withdrawal of the rejection of Claims 18-20.

CONCLUSION

Claims 7-13 and 17-20 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

Customer No.: 35273

Jeanette S. Harms
Attorney for Applicants
Reg. No. 35,537

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 11, 2005.

10/11/2005 Rebecca A Baumann
Date Signature: Rebecca A. Baumann